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METHOD AND SYSTEM OF WIRE BONDING USING INTERPOSER PADS

Cross Reference to Related Applications

This application claims priority of U.S. Provisional Patent Application No. 60/343,652 filed on December 28, 2001 entitled "Method and System of Wire Bonding Using Interposer Pads," and the teachings are incorporated herein by reference.

Technical Field of the Invention

The present invention relates to the fabrication and packaging of semiconductor devices, specifically a method and system of bonding wires from a semiconductor die to a lead using interposer pads.

Background of the Invention

Conventionally, a semiconductor die is directly connected to a lead of a semiconductor package using bonding wires. Disadvantageously, this direct connection of a bonding wire from the semiconductor die to the lead requires a wire length of less than approximately 4 mm to

maintain wire spacing from adjacent bonding wires and reduce wire shorts during encapsulation. Longer lengths of bonding wire can be used, however such use requires kinking of the bonding wire to maintain wire spacing. Kinking the bonding wires slows the fabrication of the semiconductor package.

Summary of Invention

The present invention discloses a method of wire bonding a semiconductor die to a lead using interposer pads on an electro-less substrate between the semiconductor die and the lead. This method of wire bonding allows the use of combined bonding wire lengths of up to 8 mm while reducing wire sweep, wire spacing violations and wire shorts.

Brief Description of the Drawings

For a more complete understanding of the present invention, reference is made to the following detailed description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates the conventional method of wire bonding from a semiconductor die to a lead.

Figure 2 illustrates a disclosed embodiment of the present invention.

Figure 3 illustrates the effect of kinking the bonding wire when using the conventional method of attaching the semiconductor die to the lead.

Figure 4 illustrates the elimination of the need to kink the bonding wire in the disclosed embodiment of the present invention.

Figure 5 is a top view of the semiconductor die and bonding wires comparing wire sweep using the conventional method of wire bonding and wire sweep using the disclosed embodiment of the present invention.

Figure 6 is a top view of the semiconductor die and the bonding wires frame illustrating the separation of the bonding wires in the disclosed embodiment of the present invention.

Figure 7 is a magnified, top view of an interposer pad.

Detailed Description of the Invention

Throughout the drawings, it is noted that the same reference numerals will be used to designate like or equivalent elements having the same function. Detailed descriptions of known functions and constructions unnecessarily obscuring the subject matter of the present invention have been omitted for clarity.

Figure 1 illustrates the conventional method of wire bonding from semiconductor die 10 to a stitch 14 on lead 15. One end of bonding wire 13 is attached to ball bond 12 located on semiconductor die 10. The other end of bonding wire 13 is attached to stitch 14 of lead 15. Disadvantageously, this direct connection of bonding wire 13 from semiconductor die 10 to lead 15 requires bonding wire lengths of less than approximately 4 mm to maintain wire spacing and reduce wire shorts during encapsulation.

The present invention 200 is illustrated in Figure 2. It provides a method and system of wire bonding semiconductor die 10 to lead 26 using bonding wire 20 and bonding wire 24 across

interposer pad 21. Preferably bonding wire 20 and 24 are made of a gold-based material. As used herein, gold-based means pure gold, gold-plated or a gold alloy. For purposes of clarity, Figure 2 illustrates only one of multiple semiconductor die to interposer pad to lead attachments that would be made using gold-based bonding wire on a typical semiconductor package. As illustrated therein, one end of bonding wire 20 is attached to ball bond 12 on semiconductor die 10 and the other end of bonding wire 20 is attached to interposer pad 21. One end of bonding wire 24 is attached to ball bond 23 on interposer pad 21 and the other end of bonding wire 24 is attached to stitch 25 on lead 26. The use of the present invention permits combined bonding wire lengths of up to 8 mm while reducing wire sweep, wire spacing violations and wire shorts.

As can be seen in Figure 3, if a longer length of bonding wire 13 is attached between semiconductor die 10 and lead 15 using the conventional method of wire bonding, bonding wire 13 must be kinked at one or a plurality of points (shown at 16 and 17) in order to maintain proper wire spacing. Disadvantageously, the process of kinking bonding wire 13 increases the time necessary to fabricate the semiconductor device.

As shown in Figure 4, the use of interposer pad 21 advantageously allows the combined length of bonding wires 20 and 24 to equal or exceed that of bonding wire 13 as shown in Figure 3, without the need for kinking. Fabrication times are increased because bonding wires 20 and 24 are ordinary loops without the need for special modification.

Figure 5 is a top view of semiconductor die 10 and leads 15 and 25, comparing the wire sweep of bonding wire 13 using the conventional method of wire bonding and the wire sweep of

the wires 20 and 24 using the disclosed embodiment of the present invention. As can be seen therein, the wire sweep of bonding wire 13 using the conventional technique is wider than the wire sweep of bonding wires 20 and 24 of the disclosed embodiment of the present invention. Advantageously, the narrower wire sweep of bonding wires 20 and 24 as seen in Figure 5 decreases the risk of wire spacing violations and, thus, wire shorts.

Figure 6 is a top view of semiconductor die 10, leads 15 and 65 and interposer pads 21 and 63, illustrating separation of bonding wires 20 and 61 and bonding wires 24 and 64. If interposer pad 63 is placed too close to interposer pad 21, as shown using hypothetical interposer pad 62, then potential wire to wire clearance problems arise. Advantageously, the use and placement of interposer pads 21 and 63 permits flexibility in wire to wire spacing so as to reduce or eliminate wire spacing violations and wire shorts.

The disclosed embodiment of the present invention is optimized for use in ball grid array ("BGA") packages, such as the MicroStar® BGAs fabricated by Texas Instruments. The present invention can also be used in other semiconductor packages. Preferably, the bonding wire used in the invention is gold-based. The interposer pads can be implemented using a variety of techniques with the interposer pads composed of a variety of materials, including nickel, gold, copper, carbon and aluminum. Figure 7 shows a magnified top view of a single interposer pad. As seen therein, each interposer pad 21 can have a variety of dimensions from 58 micrometers by 93 micrometers along an x-axis to 78 micrometers to 125 micrometers along a y-axis.

The numerous innovative teachings of the present application are described with particular reference to the present exemplary embodiment. However, it should be understood that this embodiment provides only one example of the many advantageous uses and innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features, but not to others.

Although an exemplary embodiment of the present invention has been illustrated in the accompanied drawings and described in this detailed description, it is understood that the invention is not limited to the embodiment disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.